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Problem 1: (25 points) Single Cycle Processor

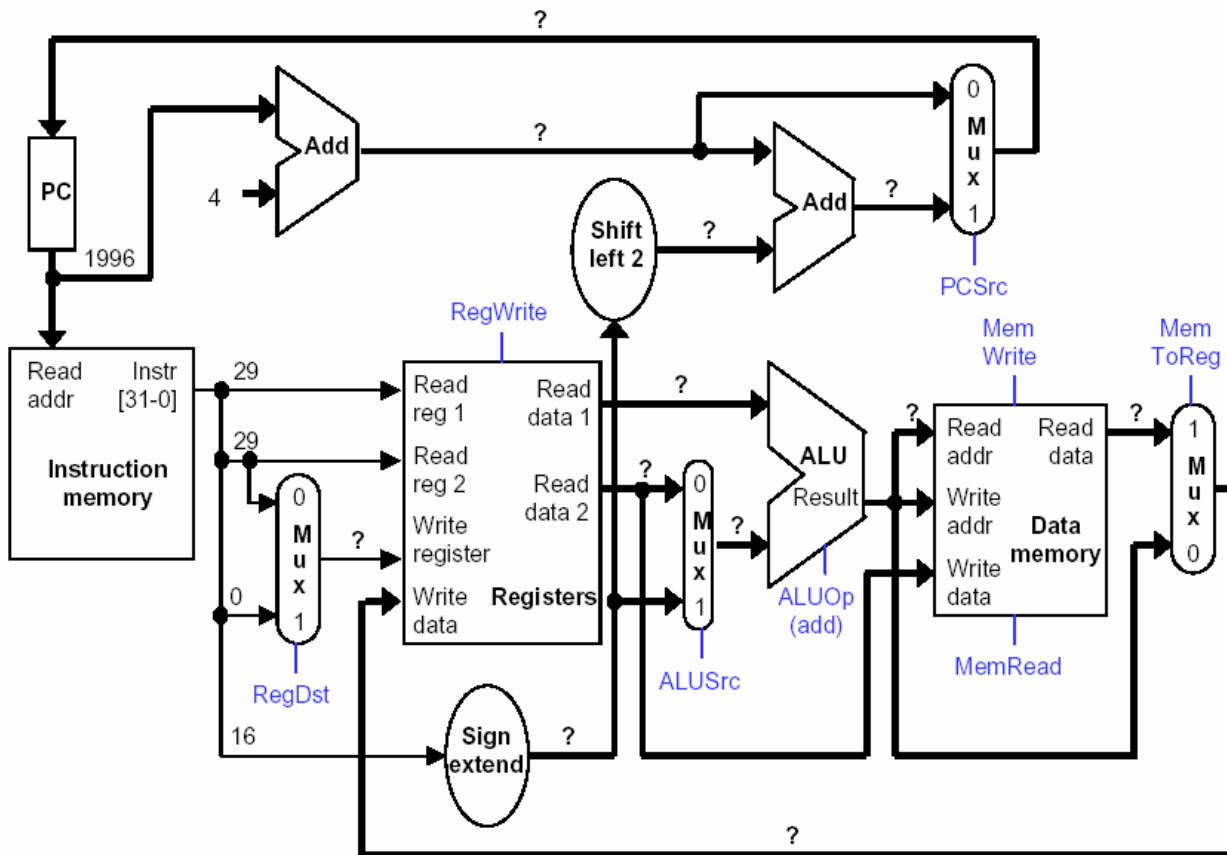
Let's say we want to execute the following immediate addition instruction in the single cycle datapath:

addi \$29, \$29, 16

The single cycle datapath diagram below shows the execution of this instruction. Several of the datapath values are filled in already. You are to provide values for the twelve remaining signals in the diagram, which are marked with a ? symbol. (2 points each)

You should:

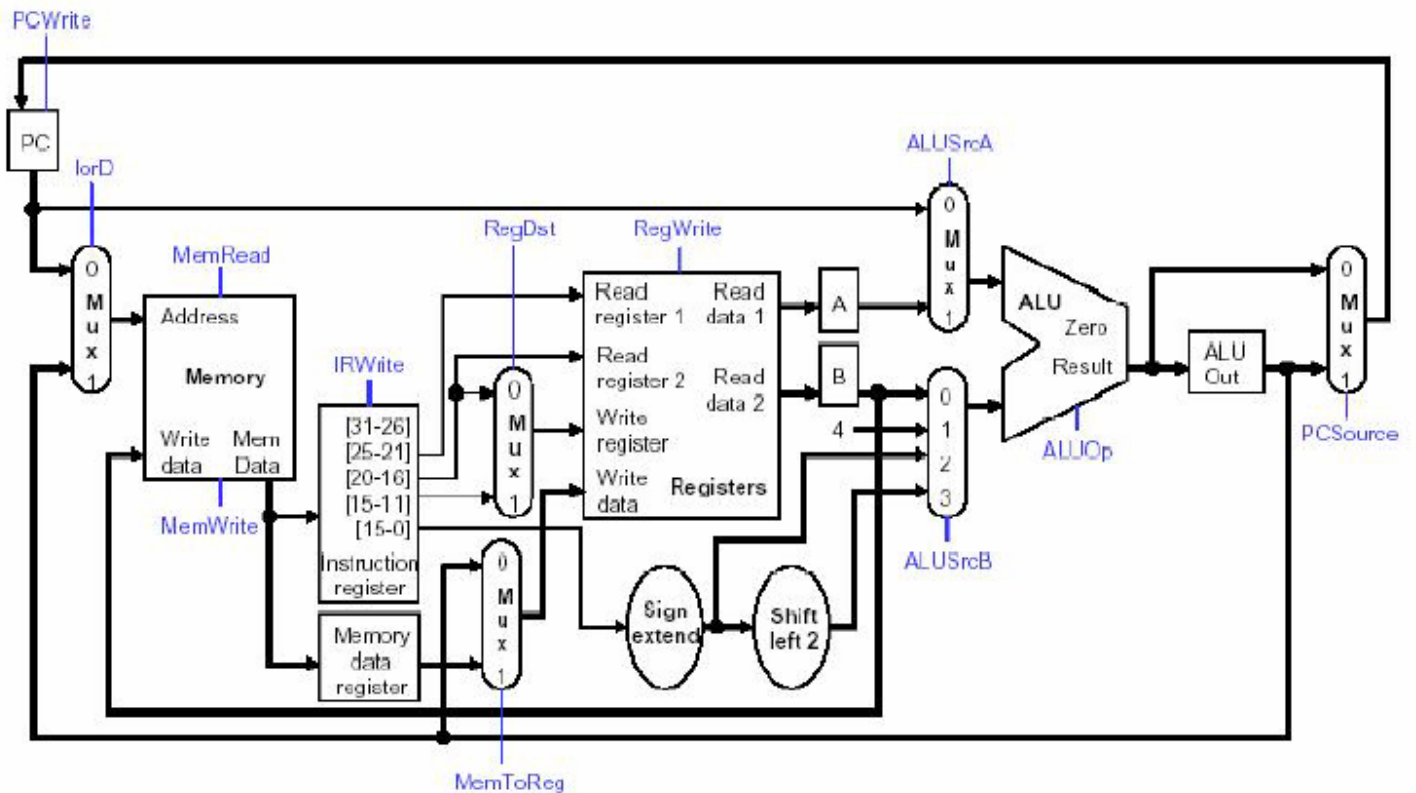
- Write your answers directly on the diagram, but write clearly.
- Show decimal values.
- Assume register \$29 initially contains the number 129.
- If a value cannot be determined, mark it as 'X.'



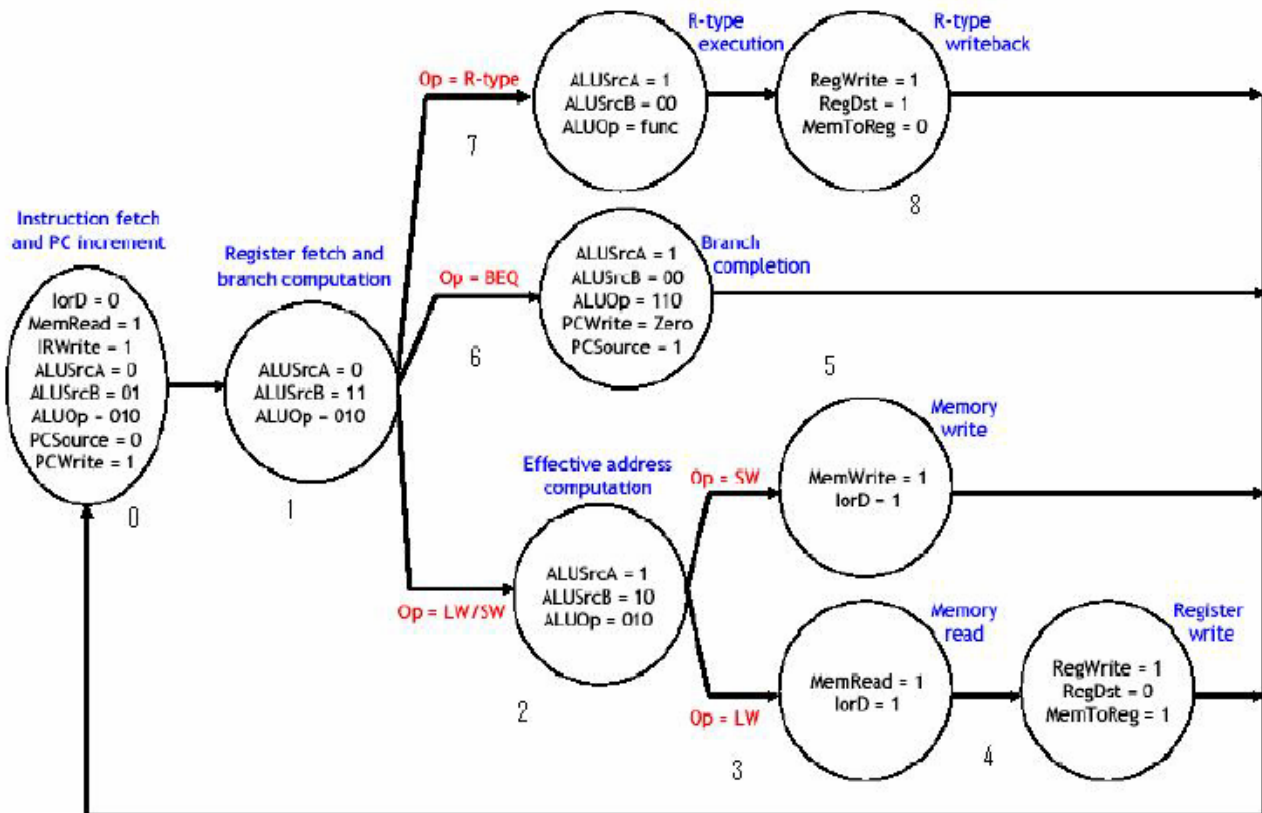
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Problem 2: (35 points) Multiple Cycle Processor

MiniMIPS is a multi-cycle implementation of MIPS supporting beq, lw, sw and R-type instructions with a single register file that has only one read port (instead of two). Show how an implementation of MiniMIPS could be obtained by modifying the datapath and finite state machine below. Your implementation must use at most five cycles per instruction!



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2. The hardware designers at MIPS have determined that the critical path that sets the clock cycle length for their multiple cycle datapath is the memory accesses for loads and stores (not for instructions). This has caused their newest processor implementation to run at a clock rate of 500 MHz rather than the target clock rate of 750 MHz. One architect came up with a solution to fix this. If every instruction that accesses memory is broken into two clock cycles, then the machine will run at the target clock rate.

a) (10 points) Using the data below, compute the CPIs for each of the implementations.

gcc data:

Instruction Class Frequency

Loads 22%
Stores 11%
R-type 49%
Jump/branch 18%

CPIs:

Instruction Class CPI on 500 MHz machine

Loads 5
Stores 4
R-type 4
Jump/branch 3

b) (10 points) The CTO of MIPS decides to implement the 750 MHz solution only if it will be faster than the 500 MHz single-cycle memory access machine on the gcc program. Will MIPS use the 500 MHz or 750 MHz machine? Why?

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$$\text{Performance} = \frac{1}{\text{Execution Time}}$$

"X is n times faster than Y" means

$$n = \frac{\text{Performance}(X)}{\text{Performance}(Y)}$$

$$\text{CPU execution time for program} \\ = \underline{\text{Instruction Count}} \times \underline{\text{CPI}} \times \underline{\text{Clock Cycle Time}}$$